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**PATENT**  
Attorney Docket No.: 015114-047930US  
Client Ref. No.: A293-D1

# 12/C  
J. BELL  
3-5-02

On Feb. 21, 2002

TOWNSEND and TOWNSEND and CREW, LLP

By: J. Matthews

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Raminda U. Madurawe et al.

Application No.: 09/606,252

Filed: June 28, 2000

For: HIGH VOLTAGE MOS DEVICES  
WITH HIGH GATED-DIODE  
BREAKDOWN VOLTAGE AND  
PUNCH-THROUGH VOLTAGE

Examiner: Paul E. Brock II

Art Unit: 2815

AMENDMENT FILED WITH RCE  
UNDER 37 C.F.R. §1.114

FAX COPY RECEIVED  
FEB 22 2002

TECHNOLOGY CENTER 2800

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

In response to the office action mailed August 21, 2001, please amend the above-identified application as follows:

03/21/2002 T20112 00000002 201430 09606252

0. 18.00 IN THE CLAIMS:

Please amend claims 27 and 38 as indicated. Please add new claim 41.

*SUB  
D1*

1 27. (Amended) A method of fabricating a transistor in an integrated  
2 circuit device comprising:  
3 providing a semiconductor substrate;  
4 forming a gate oxide on the semiconductor substrate;